Google scholar "instruction set" + decode + translate + map Search Advanced Scholar Search Scholar Preferences

Scholar Articles and patents anytime include citations Results **1** - **10** of about **6,000**. (**0.11** sec)

Shade: A fast **instruction-set** simulator for execution profiling- psu.edu [PDF]
B Cmelik, D Keppel - Proceedings of the 1994 ACM SIGMETRICS ..., 1994 - portal.acm.org
... paper describes the capabilities, design, implementation, and per- formance of Shade, and discusses **instruction set** emulation in general. **...** Shade **maps** the target PC to its corresponding **translation** using a data structure called the **Translation** Lookaside Buffer (TLB). **...**
Cited by 650 - Related articles - BL Direct - All 33 versions

Machine-adaptable dynamic binary **translation**- psu.edu [PDF]
D Ung, C Cifuentes - ACM SIGPLAN Notices, 2000 - portal.acm.org
... using dynamic **translation** techniques that were developed in Shade; a fast **instruction-set** simulator for **...** an entry exists, the corresponding target machine address is retrieved and its **translation** is fetched **...** If a match is not found, the switch manager directs the **decoding** of another **...**
Cited by 69 - Related articles - BL Direct - All 11 versions

The SimpleScalar tool set, version 2.0- psu.edu [PDF]
D Burger, TM Austin - ACM SIGARCH Computer Architecture News, 1997 - portal.acm.org
... of the tools) are: • simplesim.tar.gz - contains the simulator sources, the **instruction set** definition macros **...** in syscall, c) that intercepts system calls made by the simulated binary, **decodes** the system **...** a new platform, you will have to code the system call **translation** from SimpleScalar **...**
Cited by 1799 - Related articles - BL Direct - All 139 versions

Emulating operating system calls in an alternate **instruction set** using a modified ...
DE Richter, JC Pattin, JS Blomgren - US Patent 5,481,684, 1996 - Google Patents
... Emula- tion programs such as the SoftPC program by Insignia Corporation **translate** x86 CISC instructions **...** The dual-instruc- tion set CPU contains hardware so that it can **decode** instructions from **...** a method and apparatus to trigger a 55 switch from one **instruction set** to another **...**
Cited by 44 - Related articles - All 2 versions

... -specific processing on a general-purpose core via transparent **instruction set** ...- psu.edu [PDF]
N Clark, M Kudlur, H Park, S ... - Proceedings of the ..., 2004 - doi.ieeecomputersociety.org
... it is not clear if the algorithms extend to cover CCAs not exposed to the **instruction set**. **...** In DISE, Application Customization Functions specify how to **translate** the instruction stream of an ap- plication. **...** in a DISE implementation than in a fill unit based design, since **decode** is more **...**
Cited by 65 - Related articles - All 13 versions

... for producing a video-**instruction set** utilizing a real-time frame differential bit **map** ...
VM Shaw, SM Shaw - US Patent 5,457,780, 1995 - Google Patents
... a picturial representation of an novel integrated circuit VISC 112 (video **instruction set** computing) system **...** of internally formatted input still 10 or motion video signal and **translate** them into a **...** queuing circuit connected 2Q to the FORM 206, which receive and **decode** the presched **...**
Cited by 17 - Related articles - All 2 versions

An **instruction set** and microarchitecture for instruction level distributed processing- psu.edu [PDF]
HS Kim, JE Smith - ACM SIGARCH Computer Architecture ..., 2002 - doi.ieeecomputersociety.org
... The overall microarchitecture we propose consists of pipelined instruction fetch, **decode**, and rename stages of **...** not be a major issue (eg in some embedded systems), a new **instruction set** may be **...** A very important difference is that here the binary **translation** does not require the **...**
Cited by 88 - Related articles - BL Direct - All 28 versions

... mode control capable of supporting extensions of two distinct **instruction-set** ...
JW Goetz, SW Mahin, JJ Bergkvist - US Patent 5,854,913, 1998 - Google Patents
... Curtis, & Whitham [57] ABSTRACT A microprocessor which supports two distinct **instruction- set** architectures. **...** place under the control ol a mode bit so that the **translation** mechanism can **...** mode

Google scholar "instruction format" + recode + map Search Advanced Scholar Search Scholar Preferences

Scholar Articles and patents anytime include citations Results **1** - **10** of about **63**. (**0.17** sec)

Did you mean: "instruction format" + ***code*** + map

Feedback driven instruction-set extension- psu.edu [PDF]
U Kastens, DK Le, A Slowik, M Thies - Proceedings of the 2004 ACM …, 2004 - portal.acm.org
... instructions. In contrast to [13], [19], there is no need to **recode** the application. **...** 15]. Its specification takes the form of a tree grammar, where rules **map** fragments of intermediate language (IL) trees to sequences of target code. **...**
Cited by 18 - Related articles - BL Direct - All 7 versions

[PDF] Opcode encoding for low power embedded systems
A Pouladi, S Nooshabadi - IEEE INTERNATIONAL SYMPOSIUM …, 2005 - dsl.ee.unsw.edu.au
... Then we used a constructed code mapping to **recode** all the registers fields (Rn, Rd, and Rm **...** At this step, we **map** the condition code field (most significant nibble of the 0 **...** Schemes presented in this paper were optimized based on the data processing **instruction format** of Figure 1 **...**
Cited by 3 - Related articles - View as HTML - BL Direct - All 3 versions

Approaches to design of high level languages for microprogramming
PW Mallett, TG Lewis - International Symposium on Microarchitecture, 1974 - portal.acm.org
... (a) syntax design, (b) phase I interface design, (c) intermediate language design, (d) phase II interface design, and (e) micro- **instruction format** considerations. **...** A. goals: i. facilitate redesign and **recoding**. **...** code generator (Phase II) to **map** a low level IML into the MI target code. **...**
Cited by 3 - Related articles - All 2 versions

Am embedded system case study: the firm ware development environment for a …- psu.edu [PDF]
C Liem, M Cornero, M Santana, P Paulin, A … - Proceedings of the 34th …, 1997 - portal.acm.org
... For the code selection rules, the developer defines the **map**- ping between the C code onto the virtual machine instruction- set. **...** The **instruction format** provides orthogonal fields for parallel operations, so that compaction is rather straightforward [14]. **...**
Cited by 10 - Related articles - BL Direct - All 17 versions

[PDF] A 600-MHz VLIW DSP
S Agarwala, T Anderson, A Hill, MD Ales, R … - IEEE Journal of Solid- …, 2002 - Citeseer
... The **instruction format** resembles a 32-bit RISC instruction set with marker bits within the 32-bit **...** Instructions are **recoded** from the native 32-bit format into a 33-bit format before **...** coprocessor (TCP) is an iterative decoder that uses the maximum a posteriori (**MAP**) algorithm [3 **...**
Cited by 60 - Related articles - View as HTML - BL Direct - All 7 versions

[PDF] Conversion of an XDS Sigma-5 to a pseudo Sigma-7 or Sigma-9
WL Graves, AE Gromme, RE Melen - 1975 - slac.stanford.edu
... modified when the **instruction format** specifies that it should contain specific information. **...** that could occur before the TSTACK is initialized were **recoded** using Sigma 5 instructions. **...** mode (in which the access control is in effect though the CPU remains in master mode with **map**) **...**
View as HTML - All 3 versions

Amdahl multiple-domain architecture- princeton.edu [PDF]
RW Doran - Computer, 1988 - doi.ieeecomputersociety.org
... which domain (or mac- **recode**) is active so that it is possible to ensure that only a CPU operating on behalf of that domain is interrupted on completion of the operation. The channel processor, operating independently of the CPU, receives details of the memory **map**- ping from **...**
Cited by 6 - Related articles - All 6 versions

[BOOK] From principles of learning to strategies for instruction: empirically based …
RJ Seidel, KC Perencevich, AL Kett - 2005 - books.google.com

Page 1. FROM PRINCIPLES OF LEARNING TO STRATEGIES FOR INSTRUCTION Empirically Based Ingredients to Guide Instructional Development ROBERT J. SEIDEL KATHLEEN C. PERENCEVICH ALLYSON L. KETT Page 2. Page 3. Page 4. Page 5. **...**
Cited by 5 - Related articles

Method and apparatus for rotating active instructions in a parallel data processor

S Savkar, MC Shebanow, GW Shen, F Sajjadian - US Patent 5,838,940, 1998 - Google Patents
Page 1. United States Patent Savkar et al. US005838940A [ii] Patent Number: [45] Date of Patent: 5,838,940 Nov. 17, 1998 [54] METHOD AND APPARATUS FOR ROTATING ACTIVE INSTRUCTIONS IN A PARALLEL DATA **...**
Cited by 2 - Related articles - All 6 versions

Architecture of the IBM System/370

RP Case, A Padegs - 1978 - portal.acm.org
... (4) The time-of-day clock format contains 12 unas- signed low-order bit positions, which could be used for higher resolution. (5) A new **instruction format** was introduced for instructions that need a single operand address. The **...**
Cited by 58 - Related articles

Did you mean to search for: "instruction format" + ***code*** + map

"instruction format" + recode + map Search

Go to Google Home - About Google - About Google Scholar

©2009 Google

Google scholar "instruction format" + recode + translate + map Search Advanced Scholar Search Scholar Preferences

Scholar Articles and patents anytime include citations Results **1** - **10** of about **43**. (**0.13** sec)

Approaches to design of high level languages for microprogramming
PW Malett, TG Lewis - International Symposium on Microarchitecture, 1974 - portal.acm.org
... design, (c) intermediate language design, (d) phase II interface design, and (e) micro- **instruction format** considerations. ... MI FORMATS: A. goals: i. facilitate redesign and **recoding**. ... Producing an IML allows a target machine independent Phase I **translation**. ...
Cited by 3 - Related articles - All 2 versions

Feedback driven instruction-set extension- psu.edu [PDF]
U Kastens, DK Le, A Slowik, M Thies - Proceedings of the 2004 ACM ..., 2004 - portal.acm.org
... In contrast to [13], [19], there is no need to **recode** the application. ... stack frames larger than 32 bytes may reserve additional registers as auxiliary frame pointers for efficient **translation**. ... Its specification takes the form of a tree grammar, where rules **map** fragments of intermediate ...
Cited by 18 - Related articles - BL Direct - All 7 versions

Amdahl multiple-domain architecture- princeton.edu [PDF]
RW Doran - Computer, 1988 - doi.ieeecomputersociety.org
... operating independently of the CPU, receives details of the memory **map**- ping from ... for the few references for which **translation** is not bypassed by a **translation** lookaside buffer. ... Consequently, transitions between mac- **recode** and SCP are much more frequent than transitions ...
Cited by 6 - Related articles - All 6 versions

[PDF] ORTEP-III: Oak Ridge Thermal Ellipsoid Plot program for crystal structure ...
MN Burnett, CK Johnson - Report ORNL-6895, Oak Ridge National ..., 1996 - ccp14.ac.uk
... 30 3.3.1 **Instruction Format** . . . . This subroutine may be **recoded** to read any desired format. (See 4.5.) 1.2.8 Atom "Features" ... Rotate working — 503 Axis No. Rotation () — — — **Translate** reference — 504 ΔX (in.) ΔY (in.) ΔZ (in.) — — — ...
Cited by 329 - Related articles - View as HTML - All 19 versions

Architecture of the IBM System/370
RP Case, A Padegs - 1978 - portal.acm.org
... This approach was used also to ensure that all subse- quently introduced extensions, such as dynamic address **translation** and program-event recording, are compatible with the System/370 architecture as initially announced. ... (5) A new **instruction format** was introduced for ...
Cited by 58 - Related articles

[BOOK] From principles of learning to strategies for instruction: empirically based ...
RJ Seidel, KC Perencevich, AL Kett - 2005 - books.google.com
Page 1. FROM PRINCIPLES OF LEARNING TO STRATEGIES FOR INSTRUCTION Empirically Based Ingredients to Guide Instructional Development ROBERT J. SEIDEL KATHLEEN C. PERENCEVICH ALLYSON L. KETT Page 2. Page 3. Page 4. Page 5. ...
Cited by 5 - Related articles

Method and system for decoding plural incompatible format instructions
LD Larsen - 1996 - freepatentsonline.com
... This approach necessarily involves the use of a compiler or **translator** which, of course, must ... more machines to be intermixed in the instruction store without requiring extra **instruction format** bits to ... during the decoding cycle, the instruction contained in the IDR 1 is **recoded** to a ...

REDUCE/1700: A micro-coded Algebra system
ML Griss, RR Kessler - Proceedings of the 11th annual workshop on ..., 1978 - portal.acm.org
... new opcodes for the MBALM/1700, a complete BIL->MIL **translator** has not ... Choice of LISP Machine **Instruction format**: Many undecoded single byte opcodes (with subsidiary bytes ... an addition to an existing handcoded interpretive LISP system (MR-LISP), with minimal **recoding**. ...

Cited by 4 - Related articles - All 3 versions

Method and apparatus for rotating active instructions in a parallel data processor
S Savkar, MC Shebanow, GW Shen, F Sajjadian - US Patent 5,838,940, 1998 - Google Patents
Page 1. United States Patent Savkar et al. US005838940A [ii] Patent Number: [45] Date of Patent: 5,838,940 Nov. 17, 1998 [54] METHOD AND APPARATUS FOR ROTATING ACTIVE INSTRUCTIONS IN A PARALLEL DATA ...
Cited by 2 - Related articles - All 6 versions

[BOOK] From principles of learning to strategies for instruction: with, Workbook companion: ...
RJ Seidel, AL Kett, KC Perencevich - 2007 - books.google.com
Page 1. From Principles of Learning to Strategies for Instruction Robert J. Seidel Kathleen C. Perencevich Allyson L. Kett ! Authors with Workbook Companion A Needs-Based Focus on High School Adolescents Robert J. Seidel Allyson L. Kett Page 2. ...
Related articles

"instruction format" + recode + trans Search

©2009 Google

Google scholar ["instruction format" + decode + translate + ma] Search Advanced Scholar Search Scholar Preferences

Scholar Articles and patents anytime include citations Results **1** - **10** of about **855**. (**0.14** sec)

Microprogrammable instruction **translator**
DP Eldridge - US Patent 4,388,682, 1983 - Google Patents
... emulate another pro- cessor and execute from another instruction set, differ- 5 ent **decode** logic would **...** In **instruction format** 1, bits 11-14 are the data field, bits 15-17 are the opcode **...** the format delineation field 18 of the instruction register been 1, the format **translation** would have **...**
Cited by 9 - Related articles - All 2 versions

Translation buffer for virtual machines with address space match
AH Mason, JS Hall, PT Robinson, RT Witek - US Patent 5,319,760, 1994 - Google Patents
... To allow this, an "address space match" entry in the page table entry signals that the **translation** buffer content can be used when the address tag matches, even though the address space numbers do not **...** TB 22 IR **DECODE** 28 23 -26 L __ _ ^ FIG.2 ADDRESS GENERATION **...**
Cited by 29 - Related articles - All 6 versions

Successive **translation**, execution and interpretation of computer program having …
RL Sites - US Patent 5,507,030, 1996 - Google Patents
... COPY ORIGINAL PROGRAM (CISC) 81 •80 CISC-TO-RISC **TRANSLATOR** PROGRAM ANALYZER RISC CODE GENERATOR •83 TRANSLATED PROGRAM (RISC) CISC/RISC ADDRESS CONVERSION INFORMATION •82 •96 SUPLEMENTAL INPUT LINKER **MAP** FILE **...**
Cited by 30 - Related articles - All 2 versions

Virtual address **translator**
DB Bennett, LJ Slechta Jr, TO Wolff - US Patent 4,096,568, 1978 - Google Patents
... address. The **translator** is provided with circuits generating values which indicate the effi- ciency of its operation. Controls **...** 4 Page 10. US Patent June 20, 1978 Sheet 9 of 29 4,096,568 At AO **DECODER** Z3 Z2 ZI ZO Page 11. US **...**
Cited by 42 - Related articles - All 4 versions

The BSD packet filter: A new architecture for user-level packet capture- ⫸psu.edu [PDF]
S McCanne, V Jacobson - Proc. Winter'93 USENIX Conference, 1993 - usenix.org
... However, in implementation they are very different: The tree model **maps** naturally into code for a stack machine while the CFG model **maps** naturally into code for a register machine. **...** A sin- gle address **instruction format** minimizes the **decode**, while maintaining **...**
Cited by 764 - Related articles - All 78 versions

… code of selecting address in numerical sequence, **decoding** code strings, and …
RL Sites - US Patent 5,287,490, 1994 - Google Patents
... selected addresses are destina- tion addresses of previously-**decoded** execution transfer **...** ORIGINAL PROGRAM (CISC) 87 •80 CISC-TO-RISC **TRANSLATOR** PROGRAM ANALYZER **...** ADDRESS CONVERSION INFORMATION •82 -96 SUPLEMENTAL INPUT LINKER **MAP** RLE **...**
Cited by 26 - Related articles - All 2 versions

[PDF] ⫸Liquid SIMD: Abstracting SIMD hardware using lightweight dynamic mapping
N Clark, A Hormati, S Yehia, S Mahlke, K Flautner - Proc. of the 13th …, 2007 - Citeseer
... First, an of- fline phase takes SIMD instructions and **maps** them to an equivalent representation. Second, a dynamic **translation** phase turns the scalar representation back into architecture- specific SIMD equivalents. Fetch **Decode** Execute Retire uCode Cache SIMD Accelerator **...**
Cited by 7 - Related articles - View as HTML - All 10 versions

[PDF] ⫸A compact intermediate format for SimICS
P Magnusson, D Samuelsson - 1994 - Citeseer
... CPU ptr **decoded** instruction interpreter not_decoded **...** After gathering statistics, the simulator determines that this inner loop is suitable for **translation**. **...** The remaining registers are used as

scratch registers by the generated code to locally **map** target registers to host registers. 13 **...**
Cited by 8 - Related articles - View as HTML - All 9 versions

Delft-java dynamic **translation**- ▶ stumbleon.net (PDF)
J Glossner, S Vassiliadis - Proceedings of the 25th EUROMICRO ... - doi.ieeecomputersociety.org
... to a fixed length however all of the opcodes in the JVM are 8-bits[7]. This allows for efficient **decoding** of instructions **...** The source operand 2+ix implies that an immediate value of 2 (which is specified in the **instruction format**) is pre **...** Figure 2 shows the indirect mapping **translation**. **...**
Cited by 18 - Related articles - All 51 versions

Virtual address **translator**
LD Anderson, TO Wolff, LJ Slechta Jr - US Patent 4,084,226, 1978 - Google Patents
... The **translator** is provided with circuits generating values which indicate the effi- ciency of its operation. **...** US Patent April 11, 1978 Sheet 9 of 29 4,084,226 H CONTROL STORE 30 TS03 29# 52/j 529 Al AO **DECODER** Z3 Z2 Zl ZO A! AO EN **DECODER** Z3 72 Zl ZO ^^^^n ^^^^i " **...**
Cited by 27 - Related articles - All 4 versions

"instruction format" + decode + trans Search

©2009 Google

Google scholar "instruction format" + translate + mapping Search Advanced Scholar Search Scholar Preferences

Scholar Articles and patents anytime include citations Results **1 - 10** of about **1,470**. (**0.14** sec)

Accelerated instruction **mapping** external to source and target instruction streams ...
DE Fisk, RL Griffith, ME Homan, G Radin, WJ ... - US Patent ..., 1986 - Google Patents
... The target **instruction format** includes an nating in said CPU. **...** in a sub- routine mode whenever a sequence of source instruc- tions do not require register space **mapping**. **...** the target machine is asked to execute an instruction which indi- cates the resumption of **translation** mode. **...**
Cited by 25 - Related articles - All 7 versions

Microprogrammable instruction **translator**
DP Eldridge - US Patent 4,388,682, 1983 - Google Patents
... Because the field of interest is three bits, the **map** control bits on lines 26 would be 100 which **...** 1 can be used to **translate** a field of interest in an instruction from a predetermined 20 instruction **...** Opcode Mode Field Field Field 0 03 02 »1 00 A2 A| 1 AO **Instruction Format** 0 Format **...**
Cited by 9 - Related articles - All 2 versions

Delft-java dynamic **translation**- ⮞ stumbleon.net [PDF]
J Glossner, S Vassiliadis - Proceedings of the 25th EUROMICRO ... - doi.ieeecomputersociety.org
... The source operand 2+ix implies that an immediate value of 2 (which is specified in the **instruction format**) is pre- incremented **...** is used as the offset for all operands when the D ELFT -J AVA processor is in J AVA **translation** mode. Figure 2 shows the indirect **mapping translation**. **...**
Cited by 18 - Related articles - All 51 versions

Successive **translation**, execution and interpretation of computer program having ...
RL Sites - US Patent 5,507,030, 1996 - Google Patents
... COPY ORIGINAL PROGRAM (CISC) 81 •80 CISC-TO-RISC **TRANSLATOR** PROGRAM ANALYZER RISC CODE GENERATOR •83 TRANSLATED PROGRAM (RISC) CISC/RISC ADDRESS CONVERSION INFORMATION •82 •96 SUPLEMENTAL INPUT LINKER **MAP** FILE **...**
Cited by 30 - Related articles - All 2 versions

Translation buffer for virtual machines with address space match
AH Mason, JS Hall, PT Robinson, RT Witek - US Patent 5,319,760, 1994 - Google Patents
... 7,1994 [54] **TRANSLATION** BUFFER FOR VIRTUAL MACHINES WITH ADDRESS SPACE MATCH [75] Inventors: Andrew H. Mason, Hollis, NH; Judith S. Hall, Sudbury, Mass.; Paul T. Robinson, Arlington, Mass.; Richard T. Witek, Littleton, Mass. **...**
Cited by 29 - Related articles - All 6 versions

A multi-user data flow architecture
FJ Burkowski - Proceedings of the 8th annual symposium on ..., 1981 - portal.acm.org
... We will discuss the general features and advantages of the **instruction format** by describing the functional use and associated design aspects of the successive fields in the cell header (Figure 3): **... TRANSLATE** LOGICAL PAGE ADDRESS: This is the **mapping** operation that is **...**
Cited by 11 - Related articles

A design space exploration framework for reduced bit-width instruction set ...
A Halambi, A Shrivastava, P Biswas, N Dutt, A ... - Proceedings of the 15th ..., 2002 - portal.acm.org
... Using the rISA instructions to normal instructions **mapping**, the **translator** unit is generated, and is prepended to the decode unit. **...** Because of the uniform **instruction format**, the **translation** unit is very simple for this rISAdesign. **...**
Cited by 7 - Related articles - All 4 versions

Binary **translation** and architecture convergence issues for IBM System/390- ⮞ psu.edu [PDF]
M Gschwind, K Ebcioğlu, E Altman, S ... - Proceedings of the 14th ..., 2000 - portal.acm.org
... The **instruction format** of the VLIW instructions is based on a lim- ited variable length encoding, which was **...** are used to match in the TLB CAM, ie, there would typically be a **mapping** between

each **...** The TLB CAM used to perform the actual **translation** step can con- sist of a multi **...**
Cited by 15 - Related articles - All 8 versions

[PDF] Liquid SIMD: Abstracting SIMD hardware using lightweight dynamic **mapping**
N Clark, A Hormati, S Yehia, S Mahlke, K Flautner - Proc. of the 13th ..., 2007 - Citeseer
... SIMD instruc- tions are expressed using a processor's baseline scalar in- struction set, and light-weight dynamic **translation** maps the **...** We conclude that using dynamic techniques to **map** instructions onto SIMD accelerators is an effective way to improve computation efficiency **...**
Cited by 7 - Related articles - View as HTML - All 10 versions

[PDF] ... for determining branch addresses in programs generated by binary **translation**
M Gschwind - IBM Disclosures YOR819980334, 1998 - Citeseer
... Especially when the original program representation is in a variable-length **instruction format**, each byte **...** Uses of this invention are speedup of address **mapping** of branch target addresses from **...** to target machine address space for static and dynamic binary **translation**, in any **...**
Cited by 4 - Related articles - View as HTML - All 4 versions

©2009 Google

bit which is also used to simultaneously inform instruction **decode** which architecture **...**
Cited by 23 - Related articles - All 2 versions

Talisman: fast and accurate multicomputer simulation- ▶ psu.edu [PDF]
RC Bedichek - Proceedings of the 1995 ACM SIGMETRICS joint ..., 1995 - portal.acm.org
... also used in some processors to **translate** an **instruction set** that pro- grammers see **...** 4.1 **Translation** to Threaded Code Talisman does not interpret target instructions directly **...** the relationship among processor state, simulated physical memory, and the **decoded** instruction pages. **...**
Cited by 92 - Related articles - BL Direct - All 22 versions

Dual-**instruction-set** architecture CPU with hidden software emulation mode
JS Blomgren, DE Richter - US Patent 5,781,750, 1998 - Google Patents
... For example, random logic may instructions for enabling paging and segmentation address be used to **decode** the **instruction set** defined by an opcode **translation** and protection exist in CISC mode, and any **map** such as Tables 2 and 3. Opcode **maps** in Tables 2 and memory **...**
Cited by 20 - Related articles - All 2 versions

"instruction set" + decode + translate Search

©2009 Google